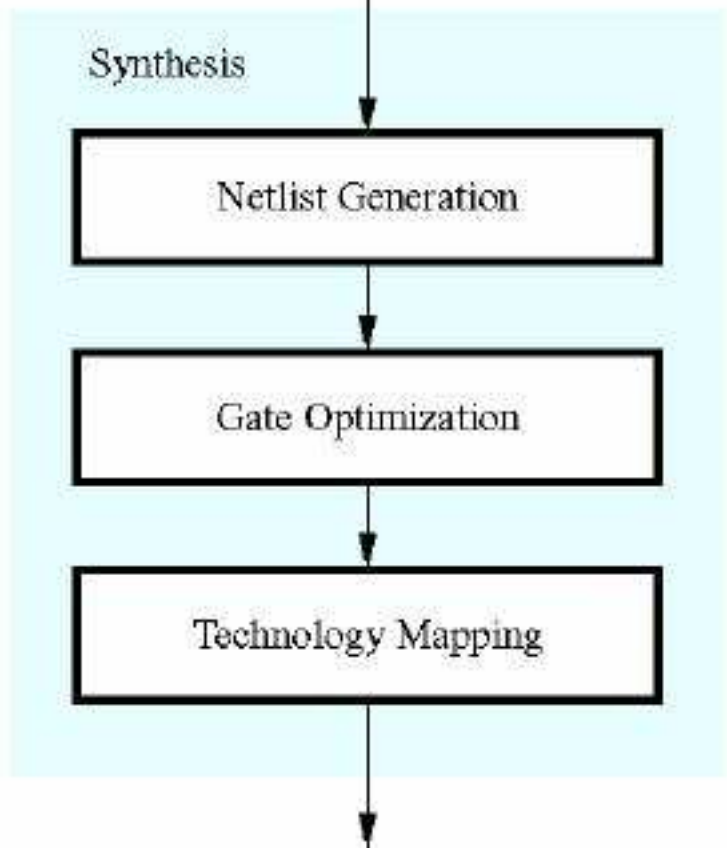


Synthesis



```
graph TD; A[ ] --> B[Netlist Generation]; B --> C[Gate Optimization]; C --> D[Technology Mapping]; D --> E[ ]
```

The diagram illustrates the Synthesis process as a vertical flowchart. It begins with an unlabeled arrow pointing down to a light blue rectangular background. Inside this background, the word "Synthesis" is written at the top. Below it, three rectangular boxes are stacked vertically, each containing a step of the process: "Netlist Generation", "Gate Optimization", and "Technology Mapping". Each box is connected to the next by a downward-pointing arrow. The final arrow points down from the bottom of the "Technology Mapping" box, extending beyond the light blue background.

Netlist Generation

Gate Optimization

Technology Mapping