

- Altera SOPC Builder
 - Create new component
 - Nios II Processor
 - SRAM_Controller**
- Bridges and Adapters
- Interface Protocols
- Legacy Components
- Memories and Memory Controllers
- Peripherals
- PLL
- University Program DE1 Board
- University Program DE2 Board
- Video and Image Processing

Target
 Device Family: Cyclone II

Clock Settings

Name	Source	MHz
clk	External	50.0

Add Remove

Use	Conne...	Module Name	Description	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>		cpu	Nios II Processor				
		instruction_master	Avalon Master	clk			
		data_master	Avalon Master				
		jtag_debug_module	Avalon Slave				
<input checked="" type="checkbox"/>		onchip_mem	On-Chip Memory (RAM or ROM)				
		s1	Avalon Slave	clk	0x00088000	0x0008ffff	
<input checked="" type="checkbox"/>		jtag_uart	JTAG UART				
		avalon_jtag_slave	Avalon Slave	clk	0x00091000	0x00091007	
<input checked="" type="checkbox"/>		SRAM_Controller_inst	SRAM_Controller				
		avalon_slave_0	Avalon Slave		0x00000000	0x0007ffff	

Remove Edit... Move Up Move Down Address Map... Filter...

Warning: SRAM_Controller_inst.avalon_slave_0: Signal "SRAM_DQ" has unknown type "export".
 Warning: SRAM_Controller_inst.avalon_slave_0: Signal "SRAM_ADDR" has unknown type "export".
 Warning: SRAM_Controller_inst.avalon_slave_0: Signal "SRAM_CE_N" has unknown type "export".
 Warning: SRAM_Controller_inst.avalon_slave_0: Signal "SRAM_YVE_N" has unknown type "export".
 Warning: SRAM_Controller_inst.avalon_slave_0: Signal "SRAM_OE_N" has unknown type "export".