Time-To-Market

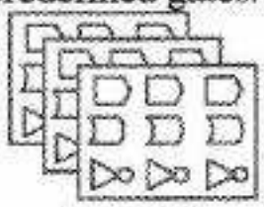
Programmable Logic Device

START
Designers obtain a premade chip, and program portions of the chip to execute the desired functionality.

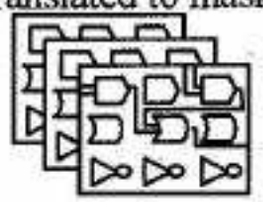
Semi-custom

Gate array

Designers are provided with a set of masks of predefined gates.



START
Designers provide the connections among gates, which are translated to masks.

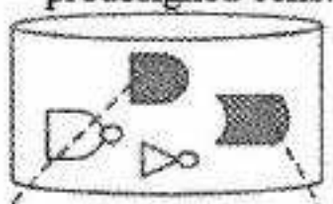


The masks are sent to the fabrication plant to produce ICs.

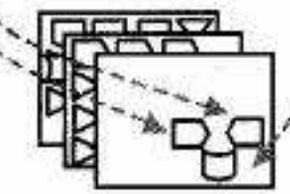
ICs are now ready to be tested/used.

Standard cell

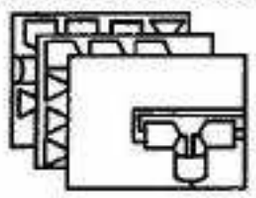
Designers are provided with a library of predesigned cells.



START
Designers choose cells, place and connect them, resulting in masks.



Designers provide the connections among cells, which are translated to masks.



The masks are sent to the fabrication plant to produce ICs.

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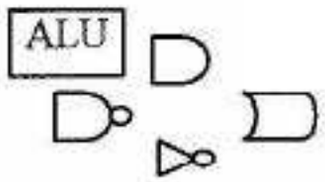
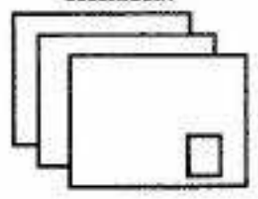
Full-custom

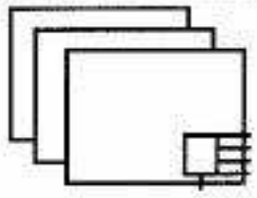
START
Designers create layouts for basic con



Designers place the components, resulting in masks.



Designers provide the connections among components, which are translated to masks.



The masks are sent to the fabrication plant to produce ICs.

ICs are now ready to be tested/used.