Name: ....
Student Number ....

Software Engineering 4A03

DAY CLASS — Dr. Mark Lawford
DURATION OF EXAMINATION: 3 Hours
McMaster University Final Examination — December 2002

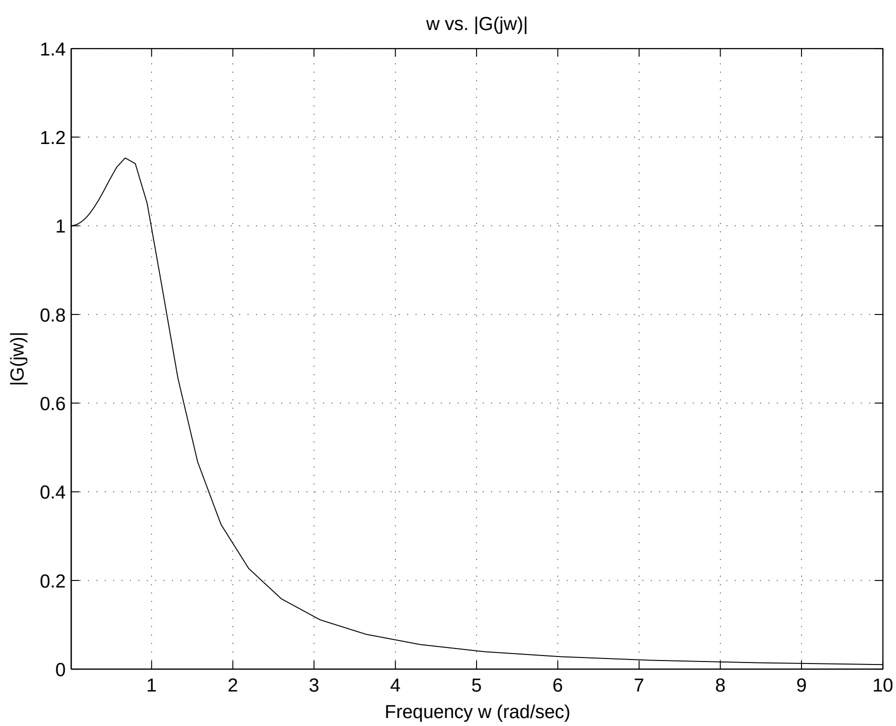
THIS EXAMINATION PAPER INCLUDES 5 PAGES AND 5 QUESTIONS. YOU ARE RESPONSIBLE FOR ENSURING THAT YOUR COPY OF THE PAPER IS COMPLETE. BRING ANY DISCREPANCY TO THE ATTENTION OF YOUR INVIGILATOR.

Special Instructions: The use of your course notes and any text books of your choice are permitted during this exam. You may use any calculator. Answer all questions in the provided answer booklets. Fill in your name and student number and sign each booklet you use. This paper must be returned with your answers.

1. Discrete Equivalents, Frequency Response & the Sampling Theorem (35 Total Marks)

a) (5 marks) Compute the discrete equivalent for $G(s) = \frac{1}{s^2+s+1}$ using the trapezoid integral approximation with period $T = 2$.

b) (3 marks) The bode plot magnitude for $G(s) = \frac{1}{s^2+s+1}$ is:



Note that $|G(-j\omega)| = |G(j\omega)|$. We can see that $G(j\omega)$ effectively acts as a low pass filter. From the graph, what is the approximate bandwidth ω_{bw} of this filter?

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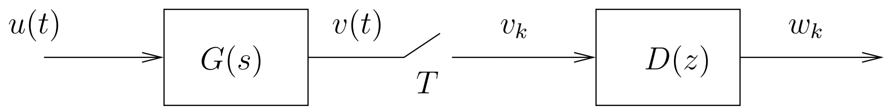

Figure 1: Diagram for Question 1

c) (7 marks) Consider Figure 1. Assume the sampling period $T = \frac{\pi}{2}$ seconds and

$$u(t) = \sin(t),\ G(S) = \frac{1}{s^2 + s + 1} \text{ and } D(z) = \frac{z}{z+1}$$

Consider only the **steady state** behaviour of the system

i) What is $v(t)$ in steady state?

ii) What is v_k in steady state?

iii) What is w_k in steady state?

d) (10 marks) Repeat all parts of the previous question with input $u(t)$ taken to be the 50% duty cycle shown in Figure 2.

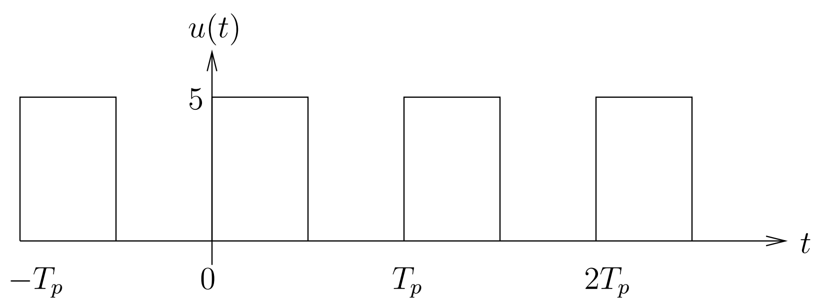

Figure 2: Graph of $u(t)$ for Questions 1

The Fourier series representation of $u(t)$ is:

$$u(t) = 2.5 + \sum_{n=0}^{\infty} \frac{10}{\pi(2n+1)} \sin\left((2n+1)\frac{2\pi}{T_p}t\right) \tag{1}$$

e) (5 marks) For $u(t)$ as given in Figure 2, sketch the spectrum $|U(j\omega)|$ and $|V(j\omega)|$ for when $T_p = \frac{2\pi}{5}$.

f) (5 marks) In theory we will have aliasing when the signal $v(t)$ is sampled to create the digital signal v_k since there are values of $\omega > \frac{\pi}{T}$ for which $|V(j\omega)| \neq 0$ (i.e. the spectrum of the sampled signal is non-zero above Nyquist frequency). Referring to your sketches in the previous part of this question, explain is this not a problem in practice if pulse period T_p is chosen so that $\frac{2\pi}{T_p} >> \omega_{bw}$.

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2. Control Systems Labs I (25 Total Marks)

For the code for the RTAI module shown below:

```
#include <linux/module.h>
#include <linux/kernel.h>
#include <linux/version.h>
#include <asm/io.h>
#include <rtai.h>
#include <rtai_sched.h>

#define PORT 0x378
RT_TASK task_data;
static int position = 0;
MODULE_PARM( position,"i");
#define TIME1ms  1000000
#define TIME9ms  9000000

void task_code( int arg) {

   RTIME nowns;

   for (;;) {
      nowns = rt_get_time_ns();

      outb(0xff,PORT);

      nowns += TIME1ms + position;
      rt_sleep_until(nano2count(nowns));

      outb(0x00,PORT);

      nowns += TIME9ms - position;
      rt_sleep_until(nano2count(nowns));
   }
}
```

a) (3 marks) What does the code do? Under "normal" (uninterrupted) operation, what is the period of the task?

b) (5 marks) Assuming the following:

- The value of `position=500000`.
- At the completion of both the first and second "periods" of the task, an interrupt that consumes 3 ms of processor time occurs between the the completion of the second `rt_sleep_until` at the end of the loop and the `rt_get_time_ns` at the beginning of the next loop.
- There are no other interruptions.

Sketch the output on a pin of `PORT` vs. time for 4 periods of the task.

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c) (5 marks) How would you modify the code to try to reduce the problems caused by the interrupt in part (b) in such a way that the code would effectively try to catch up when an interrupt occurs between the end of the execution of the current loop body and the beginning of the next loop body as describe above?

d) (5 marks) Assuming a similar interrupt pattern and other conditions as in part (b), sketch the output of a pin of `PORT` for your modified code from part (c). How does the relative jitter compare between the two versions?

e) (5 marks) Explain how the above module could be implemented using the timer in *periodic* mode instead of *one shot* mode. (NOTE: This would result in reduced resolution on output `PORT` but would use less CPU overhead for timer setup and allow the timer to be used for scheduling other periodic tasks!)

f) (2 marks) The processor load on the system has become too high. What additional hardware would allow the above task to be effectively implemented in hardware rather than software?

3. Control Systems Labs II (15 Total Marks)

The motors we used in the lab have two types of sensors that can be used to estimate the motor's angular position θ. The encoders have 1024 pulses/revolution while the potentiometer produces a voltage in the range of $[-5, +5]$ Volts that is read by a 16-bit A/D converter and translated into a measurement in the range of $[-180, +180]$ degrees. The DAQ card also has two 12-bit D/A converters to provide analog outputs. The output channel translated the range $[-360, +360]$ degrees to an output voltage in the range $[-10, +10]$ Volts.

a) (2 marks) What is the resolution in % and in degrees of the D/A conversion at the output?

b) (2 marks) In reality the potentiometer provides a voltage that has an accuracy of $\pm 0.5\%$ of what a perfect linear sensor would produce. What size error does this translate into in degrees?

c) (3 marks) Which sensor's estimate of θ is more accurate when the potentiometer's tolerance is taken into account?

d) (3 marks) In Labview we used shift registers to implement digital controllers. What is the discrete transfer function $D(z)$ from the input to the output of a shift register?

e) (5 marks) Write down a tabular description for a function to estimate the angular derivative $\dot{\theta}$ that deals with the "wrap around" problem caused when the 24-bit up/down counter used by the encoder rolls over.

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4. Scheduling & Design I (10 Total Marks)

Consider the following 3 independent tasks:

Task	Max. Compute Time	Period	Deadline
P_1	3	9	9
P_2	5	18	18
P_3	4	12	12

a) (5 marks) Show that a Rate Monotonic (RM) policy does not produce a feasible schedule.

b) (5 marks) Show that an Earliest Deadline First (EDF) policy produces a feasible schedule.

5. Scheduling & Design II (15 Total Marks)

You have been asked to design a nuclear reactor monitoring system.

a) (2 marks) Briefly describe the hardware you would use to implement such a system, justifying your choices.

b) (5 marks) Briefly describe some of the different software tasks involved in such a system and assign priorities to each task.

c) (5 marks) Indicate any tasks that share resources (e.g. a data array). For the task priority assignment you gave in (b), indicate whether or not the shared resources might causes priority inversion problems if a fixed priority scheduler is used.

d) (3 marks) Suppose you use RTAI to implement your system. Which tasks would you make real-time task (loaded as an RTAI module) and which tasks would you implement as a regular Linux process? Why?

"Dr. Lawford, for the course evaluations should we mark you out of 100 or out of 75?"- one of the more irreverent 4A03 students.

The End