Questa*-Intel® FPGA Edition Quick-Start

Intel® Quartus® Prime Standard Edition

Updated for Intel® Quartus® Prime Design Suite: **21.1**

Online Version
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Contents

1. Questa*-Intel® FPGA Edition Simulation Quick-Start (Intel® Quartus® Prime Standard Edition)

This document demonstrates how to simulate an Intel® Quartus® Prime Standard Edition design in the Questa*-Intel FPGA Edition simulator.

Note: This document intentionally uses basic features to accommodate requirements to simulate the design example mentioned in Open the Example Design on page 6. If you intend to use a different use case with advanced features and you need more information to simulate your design, then refer to the Questa-Intel FPGA Edition documents from Siemens* available in the `<installation directory>/questa_fe/docs/pdf_docs` directory.

Design simulation verifies your design before device programming. It involves generating simulation files, compiling simulation models, running the simulation, and viewing the results. The following steps describe this flow in detail:

1.1. Prerequisites

Both Questa-Intel FPGA Edition and Questa-Intel FPGA Starter Edition software require valid software licenses. However, the Questa-Intel FPGA Starter Edition license is free.

Downloading the Questa-Intel FPGA Edition and Questa-Intel FPGA Starter Edition Software

To download the software with individual executable files:

1. Visit the FPGA Software Download Center page.
2. Using the left-hand filter pane, perform the following steps to refine the search results:

a. Select the **Intel Quartus Prime Design Software** option. This displays three Intel Quartus Prime software editions (Pro, Standard or Lite).

b. Select the Intel Quartus Prime Standard software edition. This displays a list of supported software versions.

c. Select the operating system (Linux or Microsoft Windows*).

3. In the refined list of pages, click on the desired page to download the software.
4. Under the **Downloads** section, click the **Individual Files** tab.
5. Download the **Questa-Intel FPGA Edition (Includes Starter Edition)** software file(s) by clicking the **Download** button below each file name.

Refer to Downloading and Installing Intel FPGA Software in the *Intel FPGA Software Installation and Licensing* for additional information.

Generating the License

You can obtain a license for the Questa-Intel FPGA Edition and Questa-Intel FPGA Starter Edition software from the Intel FPGA Self Service Licensing Center (SSLC). If you do not have access to SSLC, you must first complete registering to SSLC and create an account by visiting Register for Intel FPGA Self Service Licensing Center (SSLC).

Follow these steps to generate the license:

1. Go to the Intel FPGA Self-Service Licensing Center (SSLC).
2. Select the **Sign up for Evaluation or Free Licenses** option on the menu bar.
3. In the list of products displayed, select the **Questa-Intel FPGA Starter Edition SW-QUESTA** option.
4. Under the **# of Seats** column, enter the number of seats you require.
5. Read the license terms of use.
6. Select the "I have read and agree to the terms of use of this license as listed below" check box.
7. Click **Get License**. A pop-up window displays asking you to which computer should the license be assigned. You can use one of the following options:

- **Option 1**: Click **Create a New Computer** if you want to assign the license to a new computer. You must provide information about the required hardware and license type. For information about the license type, refer to Intel FPGA Software License Types. For information about how to extract information about your computer hardware, refer to Hardware Information Required When You Request a License.
- **Option 2**: Click **Assign an Existing Computer** and search for the computer name/NIC ID that you have created previously in your **My Intel** account. To view your list of computers, use of the following options:
  - Visit the **License Assistant** and select **Regenerate License by Primary Computer ➤ View all computers and select**
  - On the SSLC menu bar, click **Computers and License Files** and select the desired option.

8. Click **Generate**. You receive an email with the license attached to your registered email address.
9. Save the `license.dat` file on your computer (for example, `~/intelFPGA_pro/LR-xxxxxx_License.dat`).

Note: Before using Questa-Intel FPGA Edition and Questa-Intel FPGA Starter Edition software, you must set an environment variable to point to the location of the license.

Setting Up the Questa-Intel FPGA Starter Edition Software License

After you receive and save the `license.dat` file on your computer, follow these instructions:

On Windows System

1. Go to **This PC**, right-click, and select **Properties**.
2. Click **Advanced System Setting**.
3. In the **Advanced** tab, select **Environment Variable**.
4. Under **System variables**, create a new variable with the name as `LM_LICENSE_FILE` and value as `<license.dat file path>`.
5. Click **OK** and restart the Questa software.

Alternatively, open a command prompt and run the following command to set up the `LM_LICENSE_FILE` environment variable:

```
setx LM_LICENSE_FILE <path_to_license_file>;%LM_LICENSE_FILE%
```

For example: `setx LM_LICENSE_FILE C:\intelFPGA\license.dat;%LM_LICENSE_FILE%`

On Linux System

Run one of the following commands in a command prompt window:

```
export LM_LICENSE_FILE=<path to license>:$LM_LICENSE_FILE
```

```
setenv LM_LICENSE_FILE "<path_to_license_file>"
```

Renewing the License

The software license expires 12 months after the date of purchase. To renew an expired license file, revisit the SSLC. You can renew a license only for the version that you purchased.

Related Information

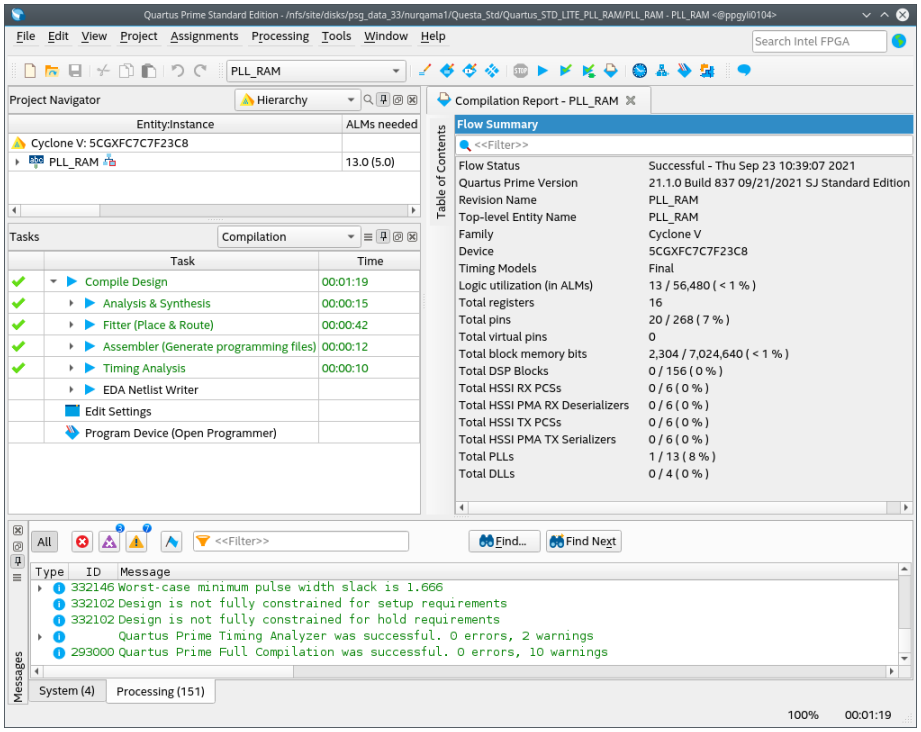
- What's New in Questa-Intel FPGA Edition
- Intel FPGA Software Installation and Licensing
- Common Licensing Q & A
- How to Get and Manage License
- Where to Get the License Daemon

1.2. Open the Example Design

The PLL_RAM example design includes Intel FPGA IP cores to demonstrate the basic simulation flow. Perform the following steps to open the design example:

1. Download and unzip the `quartus-std-lite-pll-ram` design example.
2. Launch the Intel Quartus Prime Standard Edition software version 21.1.
3. To open the example design project, click **File ➤ Open Project**, select the **pll_ram.qpf** project file, and then click **OK**.

Figure 1. `pll_ram` Project in the Intel Quartus Prime Standard Edition

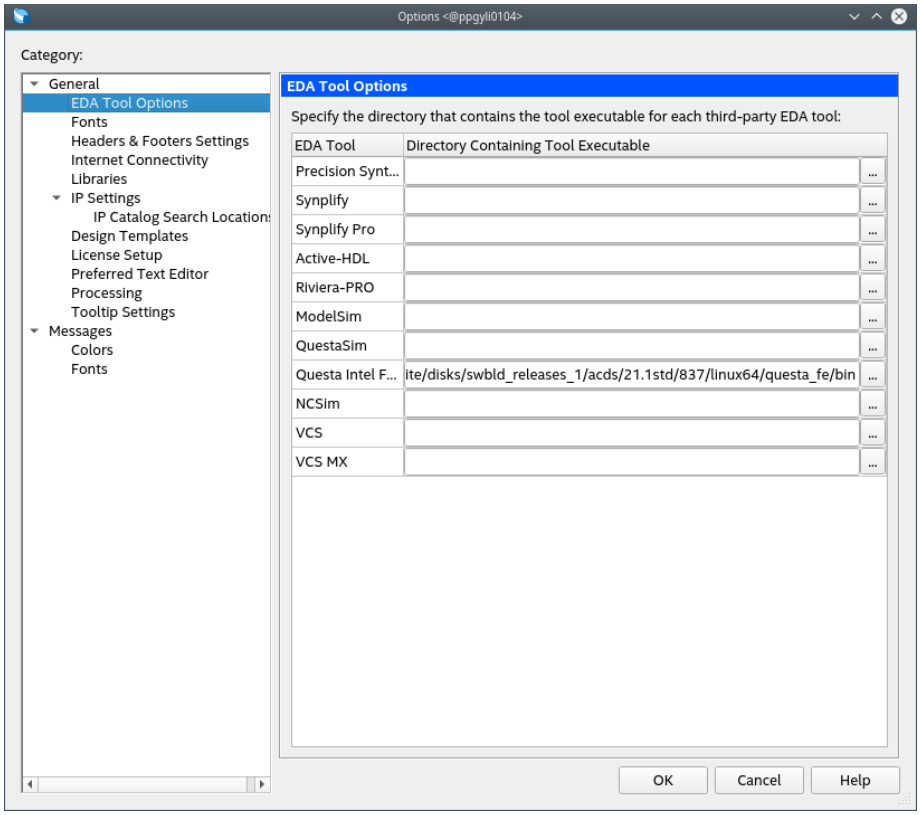


1.3. Specify EDA Tool Settings

Perform the following steps to specify EDA Tool Options and generate simulation files for the supported simulators:

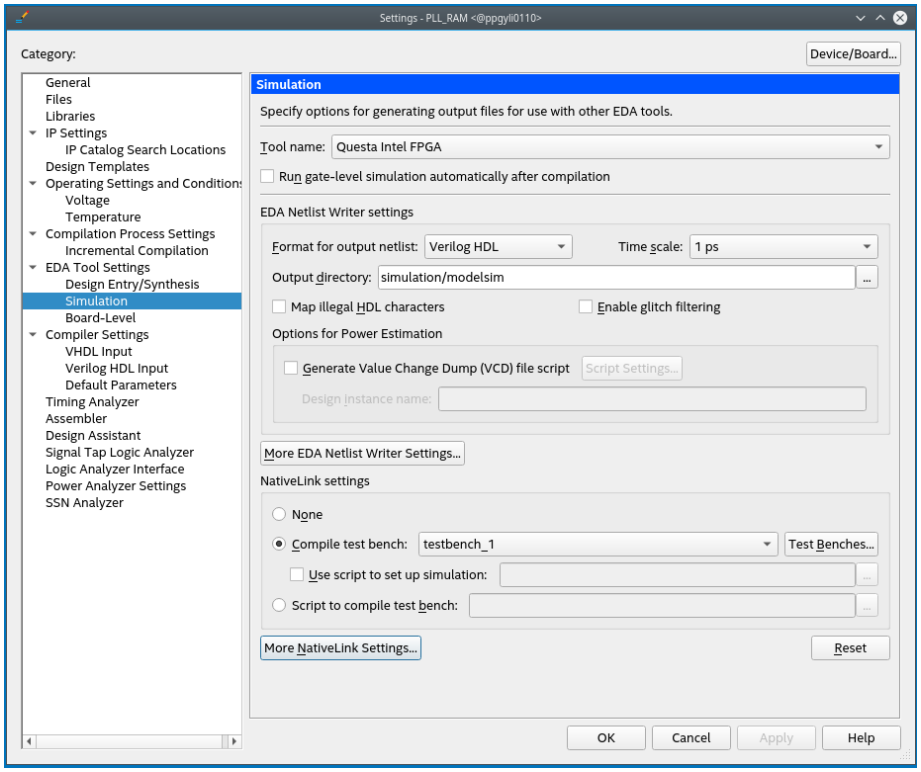
1. Click **Tools ➤ Options ➤ EDA Tool Options** to specify the location of your simulator for integration with Intel Quartus Prime Standard Edition. The **Options** dialog displays.

Figure 2. EDA Tool Settings



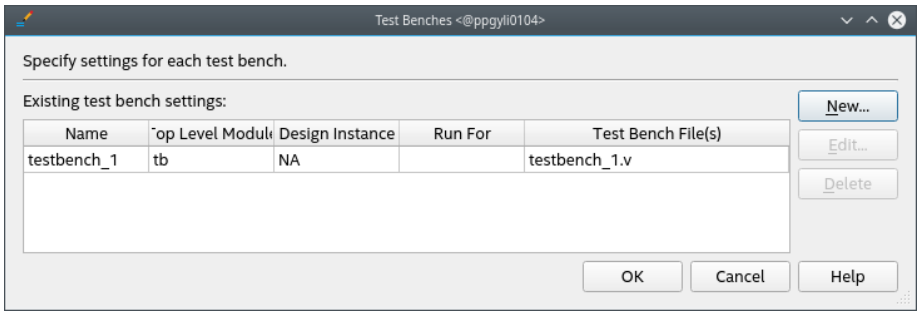
2. In the **Questa Intel FPGA** field, enter one of the following Questa-Intel FPGA Edition executable path:
   - **On Linux systems**: `<installation directory>/questa_fe/bin`
   - **On Windows systems**: `<installation directory>/questa_fe/win64`
3. Click **Assignments ➤ Settings ➤ EDA Tool Settings ➤ Simulation**. Ensure the settings are as shown in the following image:

Figure 3. Simulation Settings



4. Under **NativeLink Settings**, select the **Compile test bench** option.
5. Click the **Test Benches** button.
6. Click the **New** option to create a new test bench.
7. Specify `testbench_1` as the test bench name and `tb` as the top-level module in the test bench.
8. Under **Test bench and simulation files**, enter or select `testbench_1.v` file, click **Add**, and then click **OK**. The **Test Benches** dialog displays the properties of the test benches in your project.

Figure 4. Test Benches Dialog



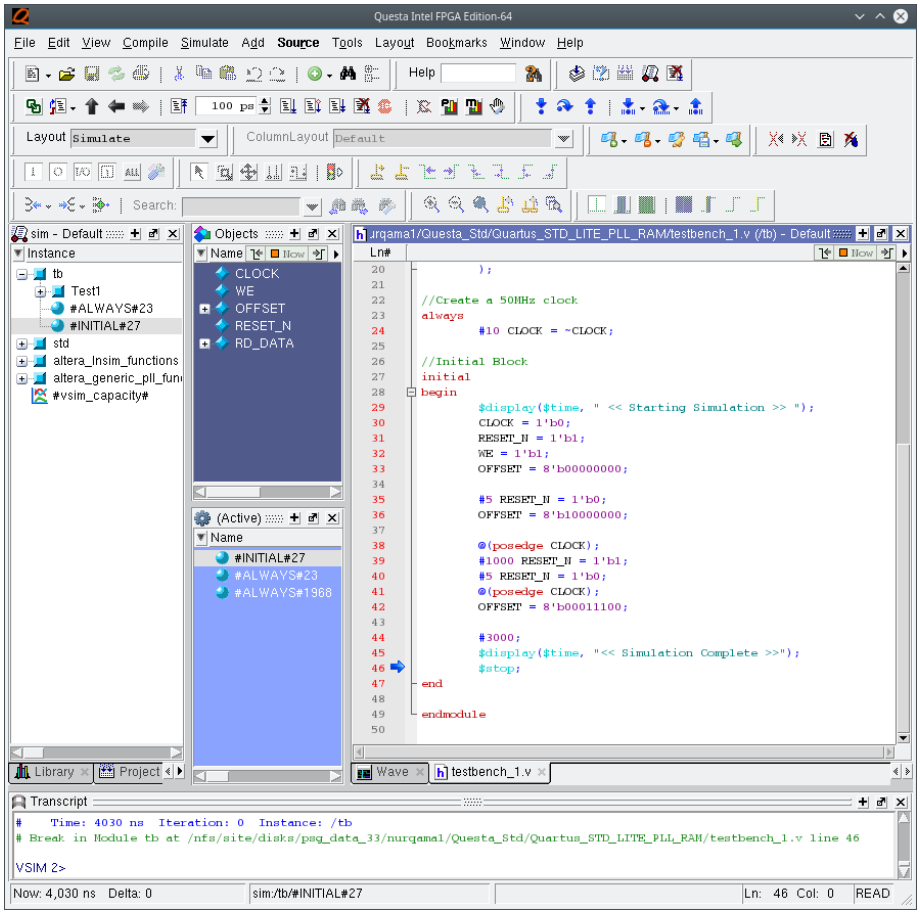
9. Click **OK** to exit **Test Benches** and **Settings** dialogs.

1.4. Launch Simulation

To generate and run Questa-Intel FPGA Edition automation script from within the Intel Quartus Prime Standard Edition software, follow these steps:

1. Click **Processing ➤ Start Compilation** to compile the design and generate the `.do` file. The **Messages** window indicates when compilation is complete.
2. Click **Tools ➤ Run Simulation Tool ➤ RTL Simulation**. The Intel Quartus Prime Standard Edition software launches the Questa-Intel FPGA Edition simulator and simulates the `testbench_1.v` file, according to your specifications in the Simulation settings.

Figure 5. Questa-Intel FPGA Edition GUI

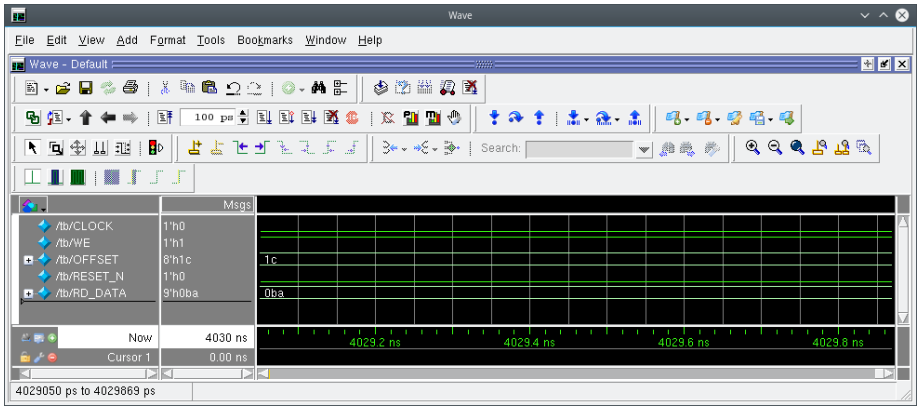


1.5. View Signal Waveforms

Follow these steps to view signals in the `testbench_1.v` simulation waveform:

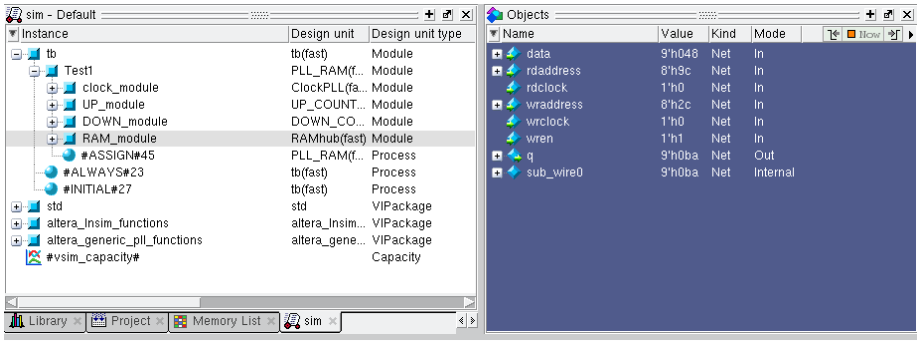
1. Click the **Wave** window. The simulation waveform ends at 11030 ns, as the testbench specifies. The **Wave** window lists the CLOCK, WE, OFFSET, RESET_N, and RD_DATA signals.

Figure 6. Questa-Intel FPGA Edition Wave Window



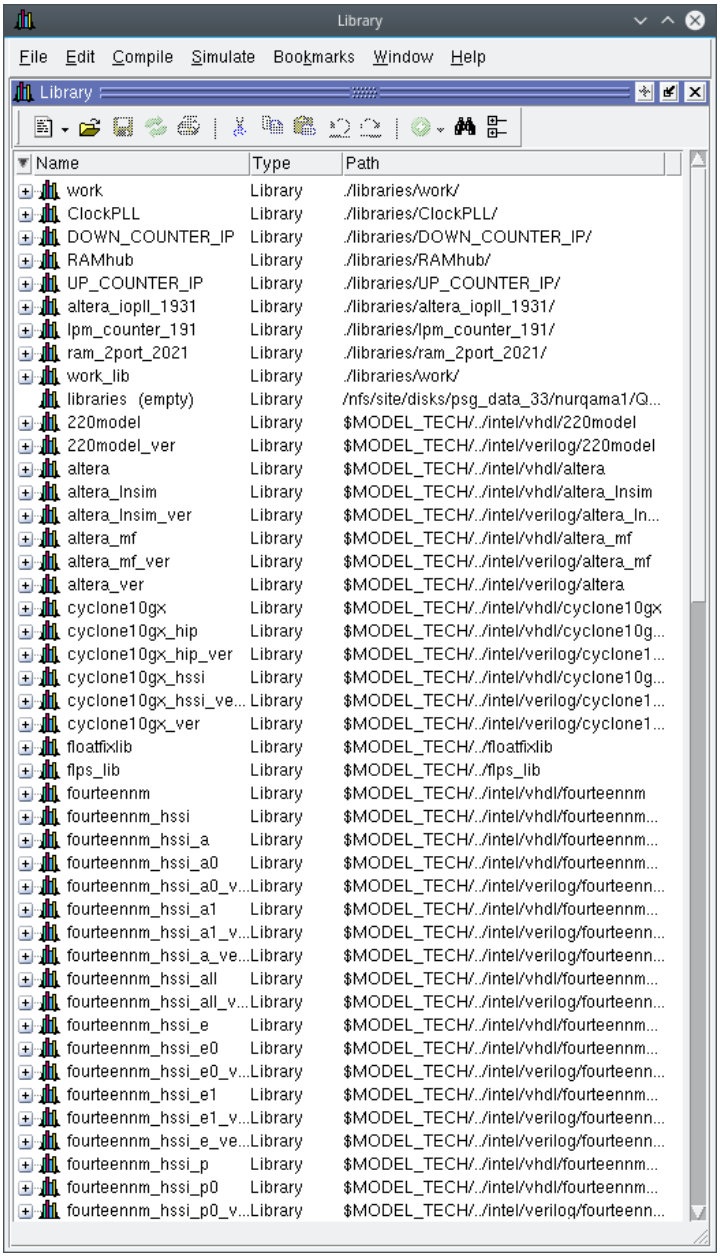
2. Click the **Sim** tab to view the signals in the top-level `pll_ram.v` design. The **Sim** window synchronizes with the **Objects** window.
3. Expand the `tb` folder in the **sim** tab to view the top-level module signals.
4. Expand the `Test1` folder. The **Objects** window displays `UP_module`, `DOWN_module`, `PLL_module`, and `RAM_module` signals.
5. In the **Sim** window, select a module under **Test1** to display the module's signals in the **Objects** window.

Figure 7. Questa-Intel FPGA Edition Sim and Objects Windows



6. View the simulation library files in the **Library** window.

Figure 8. Questa-Intel FPGA Edition Library Window



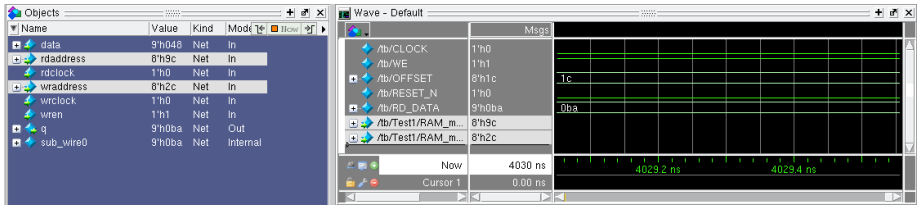
1.6. Add Signals to the Simulation

The CLOCK, WE, OFFSET, RESET_N, and RD_DATA signals automatically appear in the **Wave** window because the top-level design defines these I/O. In addition, you can optionally add internal signals to the simulation.

Perform the following steps to add signals to the simulation:

1. In the **Objects** window, locate the `UP_module`, `DOWN_module`, `PLL_module`, and `RAM_module` modules.
2. In the **Objects** window, select **RAM_module** to view the module's inputs and outputs.

Figure 9. Add Signals to the Wave Window



3. Right-click **rdaddress** and then click **Add Wave** to add the internal signals between the down-counter and dual-port RAM module.
4. Right-click **wraddress** and then click **Add Wave** to add the internal signals between the up-counter and dual-port RAM module. Alternatively, you can drag and drop these signals from the **Objects** window to the **Wave** window.
5. Click **Simulate ➤ Run ➤ Continue** to generate waveforms for the new signals you added.

1.7. Rerun Simulation

You must rerun the simulation if you make changes to the simulation setup, such as adding signals to the **Wave** window, or modifying the `testbench_1.v` file. Follow these steps to rerun simulation:

1. In the Questa-Intel FPGA Edition simulator, click **Simulate ➤ Restart**.
2. Retain the default options and click **OK**. These options clear the waveforms and restart the simulation time, while retaining the necessary signals and settings.
3. Click **Simulate ➤ Run ➤ Run -all**. The `testbench_1.v` file simulates according to the testbench specifications. To continue simulation, click **Simulate ➤ Run ➤ Continue**. This command continues the simulation until you click the **Stop** button.

2. Known Differences Between the Questa-Intel FPGA Edition and ModelSim* - Intel FPGA Edition

The following table lists major differences between the Questa-Intel FPGA Edition and ModelSim* - Intel FPGA Edition:

Table 1. Known Differences and User Actions

Known Differences		Action for Questa-Intel FPGA Edition
Questa-Intel FPGA Edition	**ModelSim - Intel FPGA Edition**	
The simulator executable path is *not* auto-populated in **Tools ➤ Options ➤ EDA Tool Options**.	The simulator executable path is auto-populated in **Tools ➤ Options ➤ EDA Tool Options**.	Follow the instructions in Specify EDA Tool Settings on page 7 to specify the executable path.
If you open an existing project with ModelSim - Intel FPGA Edition EDA tool settings, Intel Quartus Prime software replaces ModelSim - Intel FPGA Edition with Questa-Intel FPGA Edition since ModelSim - Intel FPGA Edition is no longer valid.		No action is required.
The simulator may fail during elaboration with the following message: `Error (suppressible): (vopt-14408) Intel FPGA Edition recommended capacity is 5000 non-OEM instances. There are …` This error is issued when the design capacity for the simulator is exceeded.	The same message is issued as a warning message.	Suppress this error and continue with simulation. However, the simulation runs 30X slower.
By default, the simulator does not preserve signals for waveform viewing.	Always preserves signals for waveform viewing.	Preserve signals explicitly by specifying `vsim` or `vopt` options, such as `+acc`. Refer to Add Signals to the Simulation on page 11 for more information.
The windows executable launches the simulator with the `vsim.exe` file.	The windows executable launches the simulator with the `modelsim.exe` file.	Launch the simulator with the `vsim.exe` file.
The Questa-Intel FPGA Starter Edition is free, but it requires a zero-cost license.	The ModelSim - Intel FPGA Starter Edition does not require a license.	Obtain the Questa-Intel FPGA Starter Edition license at no cost from Intel.

3. Questa-Intel FPGA Edition Quick-Start Intel Quartus Prime Standard Edition Revision History

Document Version	Intel Quartus Prime Version	Changes
2022.03.28	21.1	Added the topic *Prerequisites*.
2021.11.03	21.1	Initial release.